Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please cancel claims 1-8 without prejudice and amend claims 9, 11-23, 25, and 26 as follows:

Claims 1-8 (cancelled)

9. (currently amended): A very long instruction word (VLIW) memory system comprising:

a VLIW memory having a plurality of instruction slots for storing VLIW instruction words at addressable locations in the VLIW memory from which VLIWs may be fetched for execution;

said plurality of instruction slots comprising standard width instruction slots for storing standard width instructions and at least one ~~of said plurality of instruction slots having an~~ expanded ~~format~~ width instruction slot having a width ~~over~~ that is greater than the standard width instruction slots, the expanded width instruction slot used ~~instruction format required in program storage~~ for storing an expanded width instruction having a format that is wider than the standard width ~~instruction~~ instructions ~~width~~; and

~~means~~ the VLIW memory configured for loading said at least one expanded ~~format~~ width instruction slot with an expanded width instruction.

10. (original): The memory system of claim 9 wherein the plurality of instruction slots comprise a store unit instruction slot, a load unit instruction slot, an arithmetic logic unit (ALU) instruction slot, a multiply accumulate unit (MAU) instruction slot, and a data store unit (DSU) instruction slot.

11. (currently amended): The memory system of claim 10 wherein the store unit instruction ~~slots~~ slot is an expanded width instruction slot that ~~store~~ stores an expanded width store ~~instructions~~ instruction including additional bits to extend compute register file addressing, an additional bit to extend address register file addressing, an additional bit to expand an opcode ~~file~~field, or an additional bit to extend a conditional field.

12. (currently amended): The memory system of claim 11 wherein said ~~extended~~ expanded width store instruction ~~instructions support~~ supports expansion of a 32 x 32 bit / 16 x 64 bit configurable register file size to a 128 x 32 bit / 64 x 64 bit/ 32 x 128 bit configurable register file size.

13. (currently amended): The memory system of claim 10 where the load unit instruction ~~slots~~ slot ~~store~~ is an expanded width instruction slot that stores an expanded width load ~~instructions~~ instruction of a first format for load immediate operations including additional bits to extend compute register file addressing, a bit to extend address file register addressing, a bit to extend a conditional field or sixteen bits to extend an immediate field.

14. (currently amended): The memory system of claim 13 wherein said ~~extended~~ expanded width load instruction ~~instructions support~~ supports expansion of a 32 x 32 bit / 16 x

64 bit configurable register file size to a 128 x 32 bit / 64 x 64 bit/ 32 x 128 bit configurable register file size.

15. (currently amended): The memory system of claim 10 where the ALU, MAU and DSU instruction slots are expanded width instruction slots that store expanded width ALU, MAU, and DSU instructions including additional bits in each operand field to extend compute register file addressing, a bit to extend an opcode field, or a bit to extend a data type field.

16. (currently amended): The memory system of claim 15 wherein said ~~extended~~ expanded width ALU, MAU, and DSU instructions each ~~support~~ supports expansion of a 32 x 32 bit / 16 x 64 bit configurable register file size to a 128 x 32 bit / 64 x 64 bit/ 32 x 128 bit configurable register file size.

17. (currently amended): A very long instruction word (VLIW) instruction memory ~~(VIM)~~ basket (VIMB) system comprising:

an instruction register for storing a load indirect VLIW (LIV) instruction comprising a load mask bit field specifying which instruction slots are to be loaded in a VLIW having at least one instruction slot that is an expanded instruction slot, the VLIW accessible to be loaded at an addressable location in ~~into~~ the VIMB;

an instruction bit organizer for receiving instructions as data and based on the load mask bit field organizing the bits from the data encoded instructions into proper format for loading into the specified instruction slots in the VIMB; and

the VIMB comprising a plurality of ~~instruction slots~~VLIWs from which VLIWs may be fetched for execution, wherein the width of the at least one ~~having~~ expanded instruction slot ~~width~~ is greater than the width of ~~the instruction~~ instructions ~~format~~ required in program storage.

18. (currently amended): A very long instruction word (VLIW) memory system comprising:

an instruction memory holding a plurality of instructions ~~in a native instruction format~~ of a first bit width ~~and format~~, the plurality of instructions having at least one execute VLIW instruction; and

a very long instruction memory having instruction slots for storing instructions of ~~a second format having~~ a second bit width ~~and format~~ wherein the second bit width is different from ~~that of the native instruction format~~the first bit width and wherein the very long instruction memory holds VLIWs at addressable locations that may be fetched as a result of executing the at least one execute VLIW instruction.

19. (currently amended): The system of claim 18 wherein instructions of the second bit width are stored in a data memory and delivered to the very long instruction memory utilizing a data bus.

20. (currently amended): A very long instruction word (VLIW) memory system comprising:

a plurality of instruction slots for storing instruction words forming a VLIW, at least one of said plurality of instruction slots having a compressed format for storing a compressed instruction having a narrower instruction format with respect to an instruction format required in

~~the~~ a program storage ~~for storing a compressed instruction having narrower instruction width,~~ wherein the VLIW resides at an addressable location in a VLIW memory, the VLIW memory holding VLIWs that may be fetched for execution; and

means for loading said at least one compressed format slot with a compressed instruction.

21. (currently amended): A processing apparatus comprising:

a memory for storing a processing apparatus program comprising short instruction words;

an indirect very long instruction word (VLIW) memory comprising a plurality of instruction slots for storing instruction words, at least one of said instruction ~~slot's~~ slots having an instruction format sized according to execution function and operand storage capacity and independent of the size of the short instruction ~~word~~ words ~~size~~, wherein the plurality of instruction slots are organized to form a plurality of VLIWs and each VLIW resides at an addressable location in the indirect VLIW memory, the indirect VLIW memory holding VLIWs that may be fetched for execution;

at least one data memory unit storing instruction operands; and

at least two execution units for executing ~~the~~ a VLIW~~'s instruction words~~ fetched from the indirect VLIW memory in response to a short instruction word dispatched from the memory.

22. (currently amended): The processing apparatus of claim 21 wherein the short instruction words comprise K-bits and the ~~slot's~~ instruction format comprises T-bits, wherein T≠K.

23. (currently amended): The processing apparatus of claim 22 wherein the ~~slot's~~ instruction format comprises at least one operand address field of B-bits supporting direct operand addressing.

24. (original): The processing apparatus of claim 23 wherein the data memory unit has a capacity 2^B data values.

25. (currently amended): The processing apparatus of claim 21 wherein ~~the~~ at least one of the at least two execution units operate on a slot instruction format and directly access operands from the data memory unit for execution.

26. (currently amended): The processing apparatus of claim 21 wherein the at least two execution units operate as ~~one~~ two execution ~~unit~~ units when executing two VLIW memory slot instructions as specified by a two slot execute ~~XV~~ indirect VLIW instruction, and wherein the at least two execution units operate as one execution unit when executing one VLIW memory slot instruction as specified by a one slot execute ~~XV~~ indirect VLIW instruction.

Amendments to the Drawings:

Included in the amendment are "Annotated Sheets Showing Changes" and "Replacement Sheets" for Figs. 4B, 5B, 7B, and 14.

In Figs. 4B, 5B, and 7B correction is made to the box labeled "I" in the "d" column of the VIM 410, VIM Basket 510, and VIM Basket 710, respectively. The box labeled "I" was inadvertently labeled "I" instead of a numeric "1". The "I" has been changed to a "1" in Figs. 4B, 5B, and 7B.

In Fig. 14, line 1447 was inadvertently joined with line 1437. Both line 1447 and line 1437 separately connect to execution unit Y3i 1456, as described in the specification on page 24, lines 10-11 and lines 19-20. The joined lines have been separated and line 1447 connected to the execution unit Y3i 1456. Also, the line 1444 was inadvertently joined with line 1434. Both line 1444 and line 1434 separately connect to execution unit Y0i 1450, as described in the specification on page 24, line 9 and line 17. The joined lines have been separated and line 1444 connected to the execution unit Y0i 1450.